a very long instruction word storage **[means]** , coupled to the main memory, for receiving the very long instruction word from the main memory, and for holding the very long instruction word, the very long instruction word including a predetermined number N of individual instructions, and including at least one group of M individual instructions to be executed in parallel, where $M \leq N$, each individual instruction in the very long instruction word storage **[means]** to be executed having **[associated therewith]** a pipeline identifier indicative of **[the]** a processing pipeline for executing **[that]** the individual instruction , and having a group identifier indicative of **[the]** a group of individual instructions to which **[it]** the individual instruction is assigned for execution in parallel;

group decoder means responsive to the group identifier for each individual instruction in the very long instruction word storage to be executed for **[causing]** enabling **[all individual]** each individual instruction in the very long instruction word storage **[instructions]** having **[the same]** a similar group identifier, to be executed in parallel by the plurality of processing pipelines; and

pipeline decoder means responsive to the pipeline identifier of each **[the]** individual instructions in the **[group]** very long instruction word storage to be executed for causing each individual instruction in **[the]** a group of individual instructions having the similar group identifier to be supplied to **[an appropriate processing pipeline]** the different processing pipelines.

2. (Amended) **[A computing system as in claim 1]** The computing system in claim 1, wherein the very long instruction word storage **[means]** includes the at least one group of M individual instructions, and **[for each individual instruction the storage means]** also includes **[the]** group **[identifier]** identifiers and **[the]** pipeline **[identifier]** identifiers for each individual instruction in the at least one group of M individual instructions.

3. (Amended) **[A computing system as in claim 2]** The computing system in claim 2, wherein each individual instruction in the at least one group of M individual instructions has associated therewith a different pipeline identifier.

4. (Amended) **[A computing system as in]** The computing system of claim 1, wherein the very long instruction word storage **[means]** holds a first group of individual instructions to be executed in parallel and a second group of individual instructions to be executed in parallel after the first group, **[the]** each individual **[instructions]** instruction in **[each]** the first group having associated therewith a **[common]** first group identifier different from a second group identifier associated with each individual instruction in the second group, the first group and the second group being placed adjacent to each other in the very long instruction word storage **[means]**.

5. (Amended) **[A computing system as in]** The computing system of claim 4 wherein:

the very long instruction word storage **[means]** comprises a line in a cache memory having a fixed number of storage locations; and

the first group of individual instructions is placed at one end of the line in the cache memory, and the second group of individual instructions **[to be executed next]** is placed next to the first group of individual instructions.

6. (Amended) A method of executing in a plurality of processing pipelines arbitrary numbers of instructions in a stream of instructions in parallel which have been compiled to determine which instructions can be executed in parallel, the method comprising:

in response to the compilation, assigning a common group identifier to a group of instructions which can be executed in parallel;

determining a processing pipeline for execution of each instruction in the group of instructions to be executed;

assigning a pipeline identifier to each instruction in the group;

embedding the common group identifier and the pipeline identifier into the group of instructions; **[and]**

[placing] forming a very long instruction word with a fixed number of the instructions **[in a register, which number includes]** including at least **[one]** the group of instructions having the common group identifier as well as at least one other instruction having a different group identifier **[.]** ; and

storing the very long instruction word in a main memory.

7. (Amended) A method as in claim 6 further comprising the step of:

placing the very long instruction word retrieved from the main memory into a very long instruction word register; and

executing the group of instructions in the plurality of processing pipelines in parallel.

8. (Amended) A method as in claim 7,

wherein the very long instruction word register holds at least two groups of instructions[,] ; and

wherein the step of placing the instructions in the very long instruction word register **[for execution by the processing pipelines]** comprises placing the group of instructions **[in each group having associated therewith a common group identifier]** adjacent to **[each other]** the at least one other instruction having the different group identifier in the very long instruction word register.

9. (Amended) A method as in claim 8 wherein the step of executing **[a]** the group of instructions in parallel comprises:

coupling the very long instruction word register to a detection means to receive **[the]** group **[identifier]** identifiers of each instruction to be executed in the **[register and the group identifier of the next group of instructions to be supplied to the processing pipelines]** very long instruction word ; and

supplying only **[the]** instructions **[with]** having the **[next]** common group identifier to the processing pipelines.

10. (Amended) In a computing system having a plurality of processing pipelines in which **[a group]** groups of individual instructions, within very long instruction words, are executable in parallel by processing pipelines, a method for supplying each individual instruction in **[the]** a group to be executed in parallel to corresponding appropriate processing pipelines, the method comprising:

retrieving a very long instruction word from a main memory;

storing in a very long instruction word storage **[an instruction frame]** the very long instruction word, the **[frame]** very long instruction word including **[at least one group]** groups of individual instructions to be executed in parallel, each individual instruction **[in the group]** to be executed in the very long instruction word having **[associated therewith]** embedded therein a pipeline identifier indicative of the corresponding appropriate processing pipeline which will execute that instruction and a group identifier indicative of the group identification;

comparing the group identifier of each individual instruction in the very long instruction word **[frame with]** to an execution group identifier **[of those instructions to be next executed]** to identify an execution group; and

using the pipeline identifier of **[those]** individual instructions **[to be next executed]** in the execution group to execute each **[of the]** individual **[instructions]** instruction in the execution group in **[separate]** the corresponding appropriate processing pipelines.

11. (Amended) In a computing system having a plurality of processing pipelines in which groups of individual instructions, from a very long instruction word, are executable in parallel by **[a set of]** the plurality of processing pipelines, an apparatus for routing each individual instruction in a particular group to be executed in parallel to an appropriate processing pipeline, the apparatus comprising:

a main memory for storing the very long instruction word;

a very long instruction word storage , coupled to the main memory, for receiving the very long instruction word from the main memory and for holding **[at least one group of instructions]** the very long instruction word **[to be executed in parallel]**, the very long instruction word including groups of individual instructions, each individual instruction to be executed in the **[group]** very long instruction word storage having associated therewith a pipeline identifier indicative of **[the]** a processing pipeline for executing that individual instruction and also having associated therewith a group identifier to designate **[among the instructions present in the storage those]** a group of individual instructions to which that individual instruction is assigned **[which may be simultaneously supplied to the processing**

pipelines.] , the pipeline identifier and the group identifier embedded in the very long instruction word;

a crossbar switch having a first set of connectors coupled to the very long instruction word storage **[for transferring instructions therefrom to]** and a second set of connectors coupled to the plurality of processing pipelines;

a router coupled to the very long instruction word storage and the crossbar switch, responsive to **[the]** a pipeline identifier **[of]** for **[the]** each individual **[instructions]** instruction to be executed in the group for routing each individual **[instructions]** instruction in the group from connectors of the first set of connectors onto appropriate **[ones]** connectors of the second set of connectors, to thereby supply each individual instruction in the group to be executed in parallel to the appropriate processing pipeline.

12. **[Apparatus as in]** The apparatus of claim 11,

wherein **[:]** the first set of connectors includes a set of first communication buses, one first communication bus for each individual instruction to be executed in the very long instruction word storage;

wherein the second set of connectors includes a set of second communication buses, one second communication bus for each processing pipeline; and

wherein the router **[responsive to the pipeline identifier]** comprises:

a set of decoders coupled to the very long instruction word storage, each decoder **[to receive]** for receiving as **[a first]** input **[signal]** signals the pipeline identifier of **[a corresponding]** each individual instruction in the very long instruction word storage and in response thereto **[supply]** for supplying as output signals **[corresponding]** switch control signals corresponding to each individual instruction in the very long instruction word storage; and

a set of switches **[,]** coupled to the set of decoders and to the crossbar switch, **[to receive the switch control signals,]** one switch of the set of switches at **[the]** each intersection of each of the first set of **[connectors]** communication buses with each of the second set of **[connectors]** communication buses, **[the switches]** each switch for receiving the switch control signals and for providing connections in response to receiving

[the] a corresponding switch control signal to thereby supply each individual instruction in the group to be executed in parallel to the appropriate processing pipeline.

13. (Amended) **[Apparatus as in]** The apparatus of claim 12 further comprising:

detection means coupled to the very long instruction word storage, for **[receive]** receiving the group identifier of each individual instruction in the very long instruction word storage to be executed **[and connected to receive information regarding the next group of instructions to be supplied to the processing pipelines,]** and in response thereto supply a group control signal; and

wherein the set of decoders **[coupled to the storage]** are also coupled to the detection means **[to receive]** for receiving the group control signal and in response thereto supply **[a]** the switch control signal for only those individual instructions in the group to be supplied to the plurality of processing pipelines.

14. (Amended) **[Apparatus as in]** The apparatus of claim 13,

wherein the detection means comprises a multiplexer coupled to receive **[the]** group **[identifier]** identifiers of each individual instruction in the very long instruction word storage and **[the]** a group identifier **[of the next]** for a group of individual instructions to be next executed, and **[,]** in response thereto allow the **[next]** group of individual instructions to be supplied to the plurality of processing pipelines.

15. (Amended) Apparatus as in claim 14 wherein the multiplexer supplies **[an]** output **[signal]** signals to the set of decoders to indicate **[the]** a group identifier of **[the next]** a group of individual instructions to be next supplied to the plurality of processing pipelines.

16. (Amended) In a computing system having a plurality of processing pipelines in which **[a group]** groups of individual instructions, within a very long instruction word, are executable **[in parallel]** by the plurality of processing pipelines, each individual instruction in the very long instruction word to be executed having embedded therein a group

identifier and a pipeline identifier, an apparatus for routing each individual instruction **[in a]** of a group of individual instructions to be executed in parallel to an appropriate processing pipeline of the plurality of processing **[pipeline]** pipelines, the apparatus comprising:

a main memory for storing the very long instruction word;

a very long instruction word storage , coupled to the main memory, for receiving the very long instruction word from the main memory and for holding **[an instruction]** the **[frame]** very long instruction word **[, the frame]** the very long instruction word including **[at least one group]** groups of instructions to be executed in parallel, **[each instruction in the group having associated therewith a]** including pipeline **[identifier]** identifiers **[indicative of the processing pipeline to which that instruction is to be issued]** and **[a]** group **[identifier indicative of the group]** identifiers;

[a crossbar switch having a first set of connectors coupled to the storage for receiving instructions therefrom and a second set of connectors coupled to the processing pipelines;]

selection means coupled to the very long instruction word storage **[connected to receive]** for receiving the group **[identification]** identifier **[of]** for each individual instruction in the very long instruction **[frame and]** word, **[connected to receive]** for **[information about the group identifier of those instructions to be next executed for supplying]** determining in response thereto **[a control signal to permit the next]** a group of individual instructions to be executed in parallel, and for outputting a control signal; **[and]**

decoder means coupled to the selection means and to the very long instruction word storage, **[to receive]** for receiving the control signal and **[each of]** the pipeline **[identifiers]** identifier for each **[of the]** individual instructions in the **[storage]** very long instruction word, for **[selectively connecting ones of the first set of connectors to ones of the second set of connectors to thereby supply each instruction in the group to be executed in parallel to the appropriate processing pipeline.]** determining in response thereto the appropriate processing pipeline for each individual instruction of the group, and for outputting switch control signals;

a crossbar switch coupled to the decoder means, having a first set of connectors coupled to the very long instruction word storage for receiving the very long instruction word therefrom and a second set of connectors coupled to the plurality of

processing pipelines, for coupling each individual instruction of the group to an appropriate processing pipeline in response to the switch control signals.

17. (Amended) **[Apparatus as in]** The apparatus of claim 16,

wherein the first set of connectors **[consists of]** comprises a set of first communication buses, one first communication bus for each individual instruction held in the very long instruction word storage;

wherein the second set of connectors **[consists of]** comprises a set of second communication buses, one second communication bus for each processing pipeline;

wherein the decoder means comprises a set of decoders coupled to receive as first input signals the pipeline identifiers for each individual instruction in the group and as second input signals the pipeline identifiers for remaining individual instructions in the very long instruction word **[information about the group identifier of the next group of instructions to be executed by the pipelines and in response thereto supply corresponding switch control signals]**; and

wherein the crossbar switch **[includes]** comprises a set of switches, one switch for every **[at the]** intersection between **[of]** each of the first set of connectors **[with]** and each of the second set of connectors, **[the switches]** each switch for providing connections, in response to receiving the switch control signals, **[to thereby supply]** between each individual instruction in the group to be executed in parallel to the appropriate processing pipeline.

18. (Amended) **[Apparatus as in]** The apparatus of claim 17,

wherein the selection means **[coupled to the storage]** comprises a multiplexer coupled to receive **[each of]** the group identifiers **[of instructions]** for each individual instruction in the very long instruction word storage, and in response to **[information regarding]** the group **[identifier of the next group of instructions to be supplied to the pipelines]** identifiers, enable the **[appropriate]** decoder means to output switch control signals for each individual instructions of the group **[to be supplied to the processing pipelines]**.

19. (Amended) **[Apparatus as in]** The apparatus of claim 18,

wherein the multiplexer supplies **[an output]** a switch control signal to the **[decoders]** decoder means to **[select]** enable the decoder means to output switch control signals for each individual instruction of the group **[identifier of the next group]** of individual instructions from the very long instruction word **[to be supplied to the processing pipelines]**.

20. (Amended) In a computing system having a plurality of processing pipelines in which **[a group]** groups of individual instructions are executable, each individual instruction in a group executable in parallel by the plurality of processing pipelines, a method for transferring each individual instruction in a group to be executed through a crossbar switch having a first set of connectors coupled to **[the]** a very long instruction word storage for receiving individual instructions therefrom **[and]**, a second set of connectors coupled to the plurality of processing pipelines, and switches between the first set and the second set of connectors, the method comprising:

retrieving the very long instruction word from a main memory;

storing in the very long instruction word storage , the very long instruction word, the very long instruction word having a set of individual instructions including at least one group of individual instructions to be executed in parallel, each individual instruction in the at least one group having **[associated therewith]** embedded therein a unique pipeline identifier indicative of the processing pipeline which will execute that individual instruction, **[and]** the very long instruction word storage also including at least one other individual instruction not in the at least one group of individual instructions, **[which]** the at least one other individual instruction **[also]** having **[associated therewith]** embedded therein a different pipeline identifier; and

using the unique pipeline identifiers of the individual instructions in the at least one group of individual instructions **[which are to be executed next]** to control the switches between the first set of connectors and the second set of connectors to thereby supply each individual instruction in the at least one group to be executed in parallel to **[the]** an appropriate processing pipeline.

21. A method as in claim 20 wherein the step of using the pipeline identifiers comprises:

supplying the unique pipeline identifiers of **[the]** each individual instructions in the at least one group of individual instructions to individual **[ones]** decoders of a set of decoders, each decoder of which provides an output signal indicative of the unique pipeline identifiers of the individual instruction supplied thereto; and

using the **[decoder]** output signals of the sets of decoders to control the switches between the first set of connectors and the second set of connectors to thereby supply each individual instruction in the at least one group to be executed in parallel to an appropriate processing pipeline.

22. (Amended) A method as in claim 21 wherein each **[of the]** individual **[instructions]** instruction in the storage further includes a group identifier embedded therein to designate among the instructions present in the very long instruction word storage, which of the individual instructions may be simultaneously supplied to the plurality of processing pipelines, and the method further comprises:

supplying **[information about the]** a group identifier **[of]** for a **[the next]** group of instructions to be executed by the processing pipelines together with the group identifiers of the individual instructions in the at least one group of individual instructions to a selector;

comparing the group identifier of the **[next]** group of instructions to be executed by the processing pipelines with the group identifiers of the individual instructions in the at least one group of instructions, to provide output comparison signals; and

using both the output comparison signals and the **[decoder]** output signals to control the switches between the first set of connectors and the second set of connectors to thereby supply each instruction in the at least one group to be executed in parallel to the appropriate processing pipeline.

23. (Amended) In a computing system having a plurality of processing pipelines in which **[a group]** groups of individual instructions **[is]** are executable **[in parallel]** by the plurality of processing pipelines, a method for supplying each individual instruction in